Aurnab Mandal

130 Descanso Dr, Apt 447 San Jose, CA 95134

Education

University Of Wisconsin Madison

Masters of Science, Electrical and Computer Engineering

Madison. WI

Birla Institute Of Technology And Science, Pilani

B.E. (Hons.), Electrical And Electronics Engineering

Aug 2014—May 2019

Sep 2021—May 2023

Hyderabad, Telangana

Experience

Advantest Inc.

Jun 2023—Present

R&D Hardware Engineer

San Jose, CA

- Primary PCB designer creating board level schematics for Ultra-wide Band Phase Delay on Arrival (PDOA) module from concept to release. Responsible for bring-up and derating of Advantest custom PCAs such as instrument switching modules, RF extension modules, diagnostic loadboards, frequency up/down conversion mixers, PLL clock synthesizers.
- Assisted layout engineers through several tape-outs, ensuring high-performance and efficient designs in Siemens Xpedition. Specialized in operating Vector Network Analyzers, signal generators & analyzers, BERT.
- Developed test programs in V93k SoC ATE for fast correlation between Wave Scale RF Channel Cards (6-18 GHz) (DUT) and performance verification bench for major RF-IC manufacturers. Devised EVM measurement tests using 64-QAM, 50 MHz src modulated waveform to validate system signal integrity. Selected components such as LDO, op-amps, phase shifters, SPDT/SP4T RF Switches, RF power detectors for optimal system performance.
- Carried out compliance testing for high speed signalling and data transfer PCIe Gen 3 boards. Fine tuned a PCIe repeater by adjusting Equalizer (14.6 dB), De-emphasis (-3.5dB) settings for maximal eye opening 350-700 mV and achieved data rates up - to 8 GT/s. Used I2C, SPI serial protocols for interfacing with memory-EEPROM and DAC.

J&J Medtech Feb 2023—May 2023

Embedded Systems Co-op

Boston, MA

• Created multi threaded applications in C/C++ on an embedded real-time QNX controller to check HW-FW compatibility of Impella heart pump motor driver and AIC software. Worked with USB device drivers using BSPs.

Otsuka America Pharmaceutical Inc.

June 2022—Aug 2022

Digital Medicine Hardware Intern

Hayward, California

- Worked on physiological functions of a wearable sensor which include Ingestible sensor detection, heart rate monitoring.
- Tested and debugged a nRF52840 SoC with an ARM Cortex-M4 processor using sophisticated acoustic methods.
- Revamped an auto-regressive model to add synthetic noise at 3, 6, 9 nV/rtHz to ADC data files. Used a R-S UPV audio analyzer to study FFT, OLA STFT transforms of IEM signals. Formulated an auto-correlation function based ML model to calculate thresholds improving the efficiency of IEM sensor detection by 5%.

Projects

Sub-band Signal Analysis and Reconstruction | Signal Block Diagrams, Sub-band Coders

Jan 2022—May 2022

- Applied decimators to retain even and odd samples and examined results for aliasing of cosine signals.
- Implemented a two-band signal analysis and reconstruction system with -3dB cutoff for both high and low pass filters.

Adaptive FIR Filter Design | Active Noise Cancellation, MATLAB

Sep 2021—Dec 2021

- Designed a MMSE FIR filter with 128 taps using LMS algorithm achieving SNR of 25dB and 10dB attenuation.
- Compared SNRs to find optimum minimum step size for the algorithm to converge and implemented the filter on a TMS3206713 DSP processor.

Publications

A portable 3-D printed electrochemiluminescence platform with pencil graphite electrodes for point-of-care multiplexed analysis with smartphone-based read out

-M Salve, A Mandal, K Amreen, BP Rao, PK Pattnaik, S Goel IEEE Transactions on Instrumentation and Measurement 70, 1-10, 10 September 2020

Technical Skills

MATLAB, Python, Adobe Audition, TF32-Time Frequency Analysis Software, Siemens Xpedition, C, C++, CCStudio, LTspice, HSpice, OAI-5G, Wireshark, ADS RF, CST 3D EM Analysis